UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,753	03/10/2004	Jack Zezhong Peng	384848014US	6431

25096 7590 07/27/2005

PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,753	PENG, JACK ZEZHONG	
	Examiner	Art Unit	
	Gene N. Auduong	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-10-04, 6-14-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on March 10, 2004 and June 6, 2005 is being considered by the examiner.

Drawings

2. The drawings were received on July 7, 2004. These drawings are acceptable.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3-4, and 6-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Tang et al. (U.S. Pat. No. 6,903,984).

Regarding claim 1, Tang et al. disclose a programmable memory cell formed in a p-type semiconductor substrate and useful in a memory array (figure 3) having column bitlines and row wordlines (figure 10, column bitlines 203, 204 and row wordlines 201), the memory cell comprising: a transistor having a P+ doped gate, a gate dielectric between the gate and over the substrate (col. 2, lines 53+); and wherein the second p+ doped semiconductor region of the

transistor is connected to one of the row wordlines, and wherein the row wordline is formed by an n-type region near the surface of the semiconductor substrate (col. 2, lines 38+).

Regarding claim 3, Tang et al. disclose the memory cell of claim 1 wherein the memory cells further including a programmed doped region formed in the substrate in a channel region when the memory cell has been programmed (col. 3, lines 15+).

Regarding claim 4, Tang et al. disclose a programmable memory cell formed in an n-type well and useful in a memory array (figure 3) having column bitlines and row wordlines (figure 10, column bitlines 203, 204 and row wordlines 201), the memory cell comprising: a transistor having a n+ doped gate, a gate dielectric between the gate and over a substrate; and wherein the second n+ doped semiconductor region of the transistor is connected to one of the row wordlines, and wherein the row wordline is formed by a p-type region near the surface of the n-type well (col. 3, lines 11+; col. 2, lines 38+).

Regarding claim 6, Tang et al. disclose the memory cell of claim 4 wherein the memory cells further including a programmed doped region formed in the substrate in a channel region when the memory cell has been programmed (col. 3, lines 15+).

Regarding claim 7, Tang et al. disclose the memory cell of claim 4 wherein the n-type well is replaced by an n-type substrate (col. 3, lines 11+; col. 2, lines 38+).

Regarding claim 8, Tang et al. disclose a programmable memory cell formed in a p-type semiconductor substrate and useful in a memory array (figure 3) comprising: a plurality of column bitlines formed from p+ doped polysilicon, a dielectric between the plurality of column bitlines and over the substrate; and a plurality of row wordlines formed by n-type regions near the surface of the semiconductor substrate and intersecting with the column bitlines but separated

by the dielectric, wherein one of the memory cells is at the intersection of one of the column bitlines and one of the row wordlines (figure 10, column bitlines 203, 204 and row wordlines 201).

Regarding claim 9, Tang et al. disclose the memory cell of claim 8 wherein the memory cell further includes a programmed doped region formed in the substrate when the memory cell has been programmed (col. 3, lines 15+).

Regarding claim 10, Tang et al. disclose the memory cell of claim 8 wherein the dielectric is an oxide (col. 2, lines 53+).

Regarding claim 11, Tang et al. disclose a programmable memory cell formed in an n-type well and useful in a memory array comprising: a plurality of column bitlines formed from n+ doped polysilicon, a dielectric between the plurality of column bitlines and over a substrate; and a plurality of row wordlines formed by p-type regions near the surface of the n-type well and intersecting with the column bitlines but separated by the dielectric, wherein one of the memory cells is at the intersection of one of the column bitlines and one of the row wordlines (col. 3, lines 11+; col. 2, lines 38+).

Regarding claim 12, Tang et al. disclose the memory cell of claim 11 wherein the memory cell further includes a programmed doped region formed in the substrate when the memory cell has been programmed (col. 3, lines 15+).

Regarding claim 13, Tang et al. disclose the memory cell of claim 11 wherein the dielectric is an oxide (col. 2, lines 53+).

14. The memory cell of claim 8 wherein the n-type well is replaced by an n-type substrate (col. 3, lines 11+; col. 2, lines 38+).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tang et al. (U.S. Pat. No. 6,903,984).

Regarding claims 2 and 5, Tang et al. disclose the memory cell having all of the limitation as of claim 1. Tang et al. do not explicitly disclose wherein the gate is formed from one of the column bitlines. However, data line that connecting the gate of the memory cells can be arranged in either row direction or column direction based on the arrangement in the circuit structure and which type of memory cell being used in the circuit as shown by figures 1 and 2 of cited Takeguchi reference, U.S. Pat. No. 4,720,818. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the gate of the memory cell is formed from the column bitline direction due to the changed in type of memory cell being used for the device or changed in structure layout of the circuit to reduce space, size and cost for the device.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-14 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of U.S. Patent No. 6,777,757. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are claiming the same scope of the invention which is claiming the memory transistor having it gate connecting to the bitline and word line connecting to the source or drain region.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N. Auduong whose telephone number is (571) 272-1773. The examiner can normally be reached on 9-5-4, alternate second Monday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
July 13, 2005

Gene N Auduong
Primary Examiner
Art Unit 2827